

## Design of an Isolated 2 W Bias Supply for Telecom Systems Using the NCP1030

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### APPLICATION NOTE

#### INTRODUCTION

Power converters using secondary side controllers provide better transient response, higher efficiency and usually require less components than their primary side referenced counterparts. However, secondary side controllers require a primary side referenced bias supply to start operation. After start-up, the controller power can be provided from the secondary side.

The NCP1030 incorporates in a single IC all the active power, control logic and protection circuitry required for implementing, with a minimum of external components, a highly integrated isolated bias supply. The features included in the NCP1030 can result in a footprint area reduction by up to 91% compared to a solution implemented using discrete components.

The NCP1030 Power Switch Circuit is rated at 200 V, making it ideal for 48 V Telecom and 42 V automotive applications. In addition, this IC can operate from an existing 12 V supply. The NCP1030 includes an extensive set of features including:

- **On Board Power Switch:** Eliminates the need for an external switch. As the Power Switch characteristics are well known the gate drive is tailored to control switching transitions and help reduce electromagnetic interference (EMI).
- **An Internal Start-up Regulator:** Provides power to the NCP1030 during start-up. After start-up, the regulator is disabled, thus reducing power consumption. The regulator can be powered directly from the input line.
- **Internal Error Amplifier:** Allows the implementation of an isolated supply using primary side regulation without the need for an optocoupler.
- **Internal Cycle by Cycle Current Limit:** Eliminates the need for external sensing components. The programmed current limit is 500 mA.

- **Proprietary Active Leading Edge Blanking (LEB) Circuit:** Provides better current limit control compared to a fixed blanking period. The active LEB circuit masks the current signal during the Power Switch turn ON transition.
- **Individual Line Undervoltage and Overvoltage (UV/OV) Detectors with Hysteresis:** Eliminate the need for external supervisory function. The UV/OV detectors can be disabled if not needed.
- **Single Capacitor Oscillator:** Eliminates traditional timing resistor. Oscillator is optimized for operation up to 1.0 MHz.
- **Internal  $\pm 2\%$  Voltage Reference:** Eliminates the need for an external bypass capacitor.
- **Thermal Shutdown Circuit:** Protects the device in the event the maximum junction temperature is exceeded.

#### DESIGN SPECIFICATIONS

An isolated bias supply for a telecom system is designed and implemented using the NCP1030. The supply delivers 2.0 W at 12 V. The converter specifications are listed in Table 1.

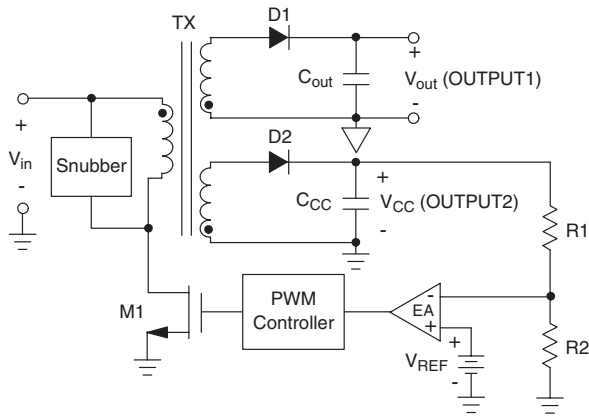
Table 1. Bias Supply Specifications

Parameter	Symbol	Min	Max
Input Voltage	$V_{in}$	35 V	76 V
Frequency	$f$	250 kHz	300 kHz
Peak Efficiency	$\eta$	80%	-
Output Voltage	$V_{out}$	10.8 V	13.2 V
Output Current	$I_{out}$	0.017 A	0.17 A
Output Power	$P_{out}$	2.0 W	-

A Flyback topology operating in discontinuous mode is selected because of its simplicity and low part count.

**FLYBACK CONVERTER**

A dual output Flyback converter is shown in Figure 1. OUTPUT 1 is regulated by means of OUTPUT 2, providing an isolated OUTPUT 1 without the need for an optocoupler.



**Figure 1. Isolated Flyback Converter**

Current flows in the primary side when the Power Switch, M1, is ON. The transformer primary side dot end becomes positive with respect to the non-dot end. While the Power Switch is ON, energy is stored in the transformer and D1 and D2 are reverse biased. When M1 turns OFF, the transformer winding polarities are reversed, forward biasing D1 and D2. Energy is transferred to the secondary outputs during this period. If the secondary current decays to zero before the switch turns ON again, the converter operates in discontinuous mode. Otherwise, it operates in continuous mode.

The converter regulates the output by sampling the output voltage and comparing it to a reference voltage. A signal proportional to their difference is generated and used to adjust the ON time of M1 such that the voltage difference is reduced.

The Snubber limits the voltage across the Power Switch and helps reduce noise.

**DESIGN PROCEDURE**

The converter is designed to operate at a maximum duty cycle (DC) of 40 % and a primary peak current (I<sub>PPK</sub>) of 400 mA. The required primary inductance, L<sub>p</sub> is calculated using Equation 1.

$$L_p = \frac{V_{in(min)} \times DC}{f \times I_{PPK}} \quad (eq. 1)$$

Solving Equation 1, a primary inductance of 127 μH is required. The transformer turns ratio  $\left(\frac{N_p}{N_s}\right)$  is calculated using Equation 2

$$\frac{N_p}{N_s} \geq \frac{(V_{in} - (I_{PPK} \times R_{DS(on)})) \times DC}{(V_{out} + V_{fD1}) \times (0.8 - DC)} \quad (eq. 2)$$

where, V<sub>fD1</sub> is the forward voltage drop across D1 and R<sub>DS(on)</sub> is the Power Switch on resistance. Equation 2 relates the on-time volt-second product to the reset volt-second product and adds a 20% dead time to insure the converter operates in discontinuous mode. Solving Equation 2 assuming a 0.5 V drop across D1,

$$\frac{N_p}{N_s} \geq \frac{(35 \text{ V} - (0.4 \text{ A} \times 7 \Omega)) \times 0.4}{(12 \text{ V} + 0.5 \text{ V}) \times (0.8 - 0.4)} \quad (eq. 3)$$

a turns ratio greater than 2.58 is required. A turns ratio of 2.78 is selected.

A maximum stress voltage of 110 V across the primary switch during the turn OFF period is calculated using Equation 4.

$$V_{stress} = V_{in(max)} + \frac{N_p}{N_s} \times (V_{out} + V_{fD1}) \quad (eq. 4)$$

The voltage is significantly below the 200 V maximum rating of the NCP1030 internal Power Switch.

The transformer winding arrangement includes a split primary with bifilar secondaries. The transformer can be ordered from Coilcraft under part number B0226-E. Table 2 summarizes the specifications of the transformer.

**Table 2. Transformer Specifications**

Parameter	Terminals	Min	Max
Magnetizing Inductance @ 0.4 A	1,2-3,4	102 μH	-
Leakage Inductance	1,2-3,4	-	0.955 μH
DC Resistance	1-4	-	0.655 Ω
	2-3	-	0.82 Ω
	5-6	-	0.248 Ω
	7-8	-	0.248 Ω
Resonant Frequency	-	3.8 MHz (typ.)	

**MAIN OUTPUT**

Two main factors, voltage ripple and frequency compensation, are considered for the selection of the output capacitor, C<sub>out</sub>. This section will focus on voltage ripple, while frequency compensation is covered in a latter section.

The output capacitor provides the load current during the switch ON time. If the target voltage droop is known, C<sub>out</sub> is calculated using Equation 5.

$$C_{out} = \frac{I_{out} \times (1 - DC)}{f \times V_{droop}} \quad (eq. 5)$$

Solving Equation 5, a maximum voltage droop of 50 mV requires a 7.4 μF capacitor. However, C<sub>out</sub> may be increased to facilitate frequency compensation.

The secondary peak current, I<sub>SPK</sub>, and the diode blocking voltage, V<sub>block</sub>, determine the selection of rectification diodes, D1 and D2.

The primary peak current and transformer turns ratio determine the secondary peak current as given by Equation 6.

$$I_{SPK} = I_{PPK} \times \frac{N_p}{N_s} \quad (eq. 6)$$

The voltage across the rectification diode is given by Equation 7.

$$V_{\text{block}} = V_{\text{out}} + V_{\text{in(max)}} \times \left( \frac{N_s}{N_p} \right) \quad (\text{eq. 7})$$

Solving Equations 6 and 7, the rectification diode needs to handle 1.11 A and 39.34 V. In addition to the voltage calculated using equation 7, voltage spikes during switching transitions need to be considered when selecting the blocking voltage rating. A Schottky diode is selected to reduce the forward voltage drop, thus reducing power dissipation. On Semiconductor's MBRA160 is selected as it meets all the requirements.

### AUXILIARY SUPPLY REGULATOR

The auxiliary supply (OUTPUT 2) provides a means to regulate the main output (OUTPUT 1). In addition, the auxiliary winding disables the internal start-up circuit and provides power to the NCP1030 after initial power up. The same turns ratio and rectification diode used for the main output are used for the auxiliary winding to improve voltage tracking between the outputs.

The auxiliary winding capacitor,  $C_{CC}$ , is selected such that a voltage greater than 7.5 V is maintained on the  $V_{CC}$  pin while the output reaches regulation. The time the output reaches regulation is measured at 0.8 ms. Once the start-up time is known,  $C_{CC}$  is calculated using Equation 8.

$$C_{CC} = \frac{I_{CC} \times t}{2.5 \text{ V}} \quad (\text{eq. 8})$$

where,  $I_{CC}$  includes the NCP1030 bias current ( $I_{CC3}$ ) and any additional current supplied by  $C_{CC}$ . Assuming an  $I_{CC3}$  of 3.0 mA and a 2.0 mA bias current for the feedback sensing resistors,  $C_{CC}$  is calculated at 1.6  $\mu\text{F}$ . The  $V_{CC}$  capacitor is set at 2.2  $\mu\text{F}$ . Please note that if  $C_{CC}$  is increased to match  $C_{\text{out}}$ , the transient response of the converter will suffer. This is because the capacitance to current ratio of the auxiliary winding is significantly greater than the output winding, taking it longer for  $C_{CC}$  to follow  $C_{\text{out}}$  during a transient condition.

### FEEDBACK LOOP

If the feedback loop is not stable, the converter will oscillate. To insure the loop is stable, the open loop frequency response needs to cross 0 dB at a slope of -20 dB/dec, with a phase margin above 45° under all line and load conditions. This is accomplished by shaping the loop response using the internal error amplifier (EA).

The block diagram shown in Figure 2 is used to evaluate the converter open loop response.

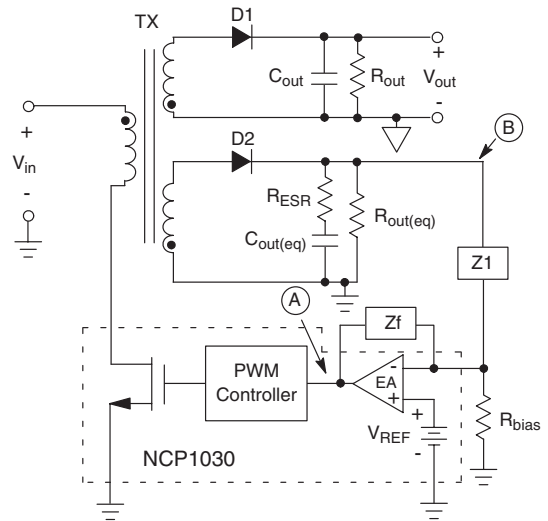


Figure 2. Flyback Converters

The open loop frequency response of the system (from A to B) is approximated by the modulator gain and the output network frequency response. Additional high frequency components are present but are not considered for our analysis as they are far beyond the crossover frequency. The modulator gain,  $G_{\text{MOD}}$ , is approximated by Equation 9.

$$G_{\text{MOD}} = \frac{3}{2} V_{\text{in}} \times \sqrt{\frac{R_{\text{out(eq)}} \times \eta}{2 \times f \times L_p}} \quad (\text{eq. 9})$$

The output network block is comprised of  $C_{\text{out}}$ ,  $R_{\text{ESR}}$  and  $R_{\text{out}}$ . The frequency response of the output network is given by Equation 10.

$$H(f) = \frac{s R_{\text{ESR}} C_{\text{out(eq)}} + 1}{s C_{\text{out(eq)}} (R_{\text{ESR}} + R_{\text{out(eq)}}) + 1} \quad (\text{eq. 10})$$

The total open loop frequency response is the product of Equations 9 and 10. Please note that  $C_{\text{out(eq)}}$  includes  $C_{CC}$  and  $C_{\text{out}}$  reflected to the auxiliary winding by the transformer turns ratio. As the same turns ratio is used for both the auxiliary and output windings,  $C_{\text{out}}$  adds directly to  $C_{CC}$ . The output network has one zero and one pole and they are given by Equations 11 and 12, respectively.

$$f_{z1} = \frac{1}{2\pi C_{\text{out}} R_{\text{ESR}}} \quad (\text{eq. 11})$$

$$f_{p1} \approx \frac{1}{2\pi R_{\text{out}} C_{\text{out}}} \quad (\text{eq. 12})$$

The modulator gain response depends on  $V_{\text{in}}$ . Two extreme conditions, both minimum  $R_{\text{out}}$  and input voltage ( $G_{\text{MOD1}}$ ) as well as both maximum  $R_{\text{out}}$  and input voltage ( $G_{\text{MOD2}}$ ) are considered for frequency compensation. In order to facilitate frequency compensation,  $C_{\text{out}}$  is increased to 22  $\mu\text{F}$ . The simulated open loop frequency responses for  $G_{\text{MOD1}}$  and  $G_{\text{MOD2}}$  are shown in Figures 3 and 4, respectively.

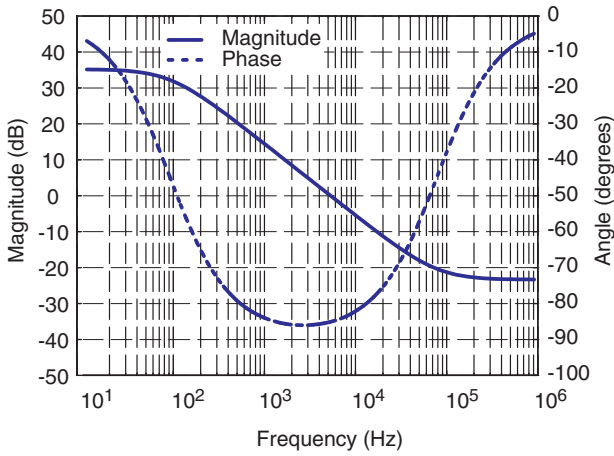


Figure 3. Open Loop Frequency Response for  $G_{MOD1}$

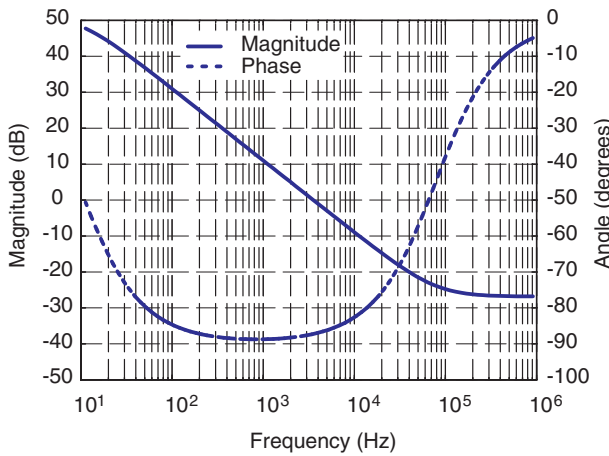


Figure 4. Open Loop Frequency Response for  $G_{MOD2}$

The frequency compensation can be achieved using a type II error amplifier (EA) as the one shown in Figure 5.

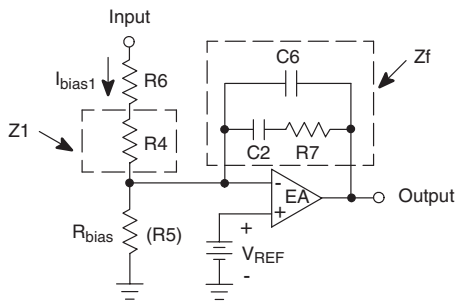


Figure 5. Type II Error Amplifier

A type II error amplifier has 2 poles and 1 zero. The transfer function is given by Equation 13.

$$H(f) = \frac{sR_7C_2 + 1}{sR_4(C_2 + C_6)(1 + sR_7\frac{C_7C_6}{C_7+C_6})} \quad (\text{eq. 13})$$

One of the poles,  $f_{p2}$ , is at the origin. The frequency of the remaining pole and zero are given by Equations 14 and 15, respectively.

$$f_{z2} = \frac{1}{2\pi R_7 C_2} \quad (\text{eq. 14})$$

$$f_{p3} = \frac{(C_2 + C_6)}{2\pi R_7 C_2 C_6} \quad (\text{eq. 15})$$

The EA poles and zero locations are selected to achieve the desired crossover frequency,  $f_{CO}$ . A system crossover frequency of 10 kHz is selected for  $G_{MOD1}$ . As the modulator gain depends on the input voltage, a higher  $f_{CO}$  is obtained for the maximum input voltage condition with equivalent output load.

The selection of the compensation components begins by noting that the voltage on the  $V_{FB}$  pin should be equal to 2.5 V ( $V_{REF}$ ) when the output is in regulation (12 V). If the feedback sensing resistor network bias current ( $I_{bias1}$ ) is known,  $R_4$  and  $R_5$  are calculated using Equations 16 and 17, respectively.

$$R_5 = \frac{V_{REF}}{I_{bias1}} \quad (\text{eq. 16})$$

$$R_4 = \frac{V_{CC}}{I_{bias1}} - R_5 \quad (\text{eq. 17})$$

Using a bias current of 2.0 mA,  $R_4$  and  $R_5$  are calculated at 4.99 k $\Omega$  and 1.30 k $\Omega$ , respectively. Resistor  $R_6$  provides a test point to measure the open loop frequency response. It is set at 10  $\Omega$  to avoid disrupting the DC bias point.

The error amplifier DC gain,  $G_{EA}$ , is calculated using Equation 18. It is set at 6.03 dB to achieve a gain of 0 dB at 10 kHz for  $G_{MOD1}$ .

$$G_{EA} = 20 \log\left(\frac{R_7}{R_4}\right) \quad (\text{eq. 18})$$

The error amplifier zero,  $f_{z2}$ , is placed before the system response crosses 0 dB. Pole,  $f_{p3}$ , is placed after  $f_{CO}$  to attenuate high frequency components. Table 3 summarizes the system gain, poles and zeros. Figure 6 shows the EA frequency response.

Table 3. System Gain, Poles and Zeros

Parameter	Frequency (kHz)	Magnitude (dB)
$f_{P1}$ (@ $G_{MOD1}$ )	0.091	-
$f_{P1}$ (@ $G_{MOD2}$ )	0.009	-
$f_{P2}$	0	-
$f_{P3}$	23.9	-
$f_{Z1}$	77.4	-
$f_{Z2}$	0.482	-
$G_{EA}$	-	6.03

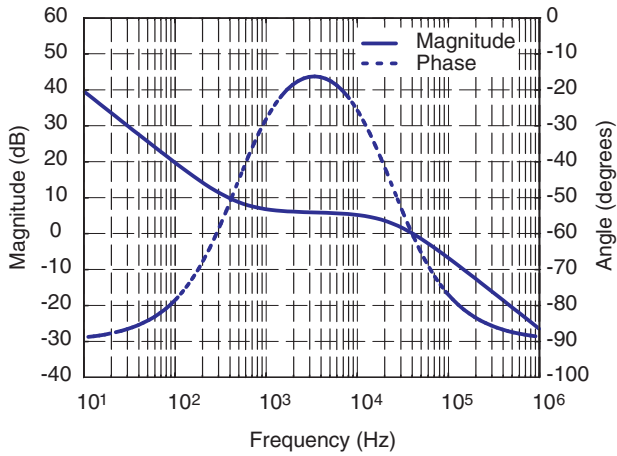


Figure 6. Error Amplifier Frequency Response

The phase contributions of a zero and a pole at the crossover frequency are given by Equations 19 and 20, respectively.

$$\theta_z = \tan^{-1}\left(\frac{f_{CO}}{f_z}\right) \quad (\text{eq. 19})$$

$$\theta_p = \tan^{-1}\left(\frac{f_{CO}}{f_p}\right) \quad (\text{eq. 20})$$

The phase margin,  $\theta_M$ , is evaluated taking into account the phase contribution of all the poles and zeros as shown below in Equation 21.

$$\theta_M^\circ = 180 - \theta_{p1} - \theta_{p2} - \theta_{p3} + \theta_{z1} + \theta_{z2} \quad (\text{eq. 21})$$

$$\theta_M = 180^\circ - 89.5^\circ - 90^\circ - 22.7^\circ + 7.33^\circ + 87.24^\circ = 72.4^\circ$$

The calculated phase margin is 72.4°. The 180° term arises because the EA is in an inverting configuration. The simulated system frequency responses for  $G_{MOD1}$  and  $G_{MOD2}$  are shown in Figure 7.

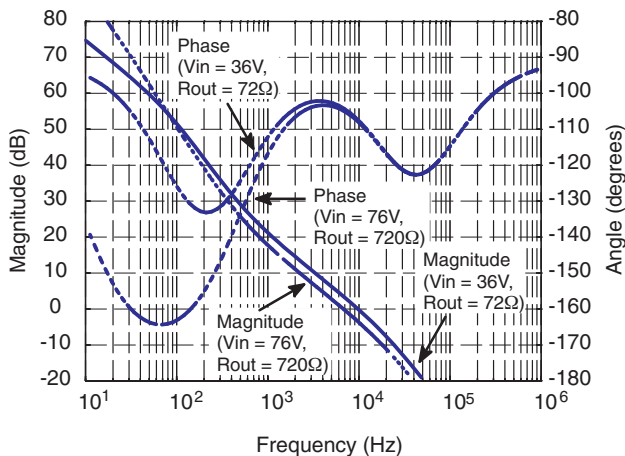


Figure 7. System Frequency Response

## UNDER/OVERVOLTAGE DETECTORS

The NCP1030 eliminates the need for additional supervisory circuitry by incorporating individual under and overvoltage detectors with hysteresis. The controller is enabled if the voltage on the UV pin is above 2.5 V and the voltage on the OV pin is below 2.5 V. The UV/OV detectors can be biased using an external resistor divider as shown in Figure 8.

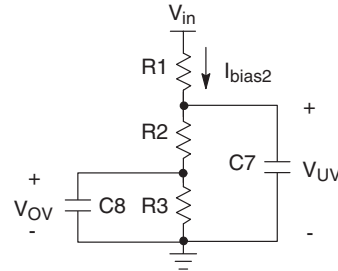


Figure 8. UV/OV Resistor Bias Network

If the resistor network bias current,  $I_{bias2}$ , is known, and the  $V_{OV}$  and  $V_{UV}$  thresholds are equal,  $R_1$ ,  $R_3$  and  $R_2$  are calculated using Equations 22, 23 and 24, respectively.

$$R_1 \approx \frac{V_{in(max)}}{I_{bias2}} \quad (\text{eq. 22})$$

$$R_3 \approx \frac{V_{OV} \times R_1 \times V_{in(min)}}{V_{in(min)}V_{in(max)} - V_{OV}(\Delta V_{in} + V_{in(min)})} \quad (\text{eq. 23})$$

$$R_2 \approx \frac{R_3 \times \Delta V_{in}}{V_{in(min)}} \quad (\text{eq. 24})$$

Using a bias current of 78  $\mu\text{A}$ , a turn ON voltage of 35 V, a turn OFF voltage of 80 V and a  $V_{OV}$  threshold of 2.55 V,  $R_1$ ,  $R_2$  and  $R_3$  are calculated at approximately 1.0 M $\Omega$ , 45.3 k $\Omega$  and 34 k $\Omega$ , respectively. Capacitors  $C_7$  and  $C_8$  help reduce noise and provide a stable voltage during turn ON and turn OFF transitions. They are set at 10 nF.

## OSCILLATOR FREQUENCY

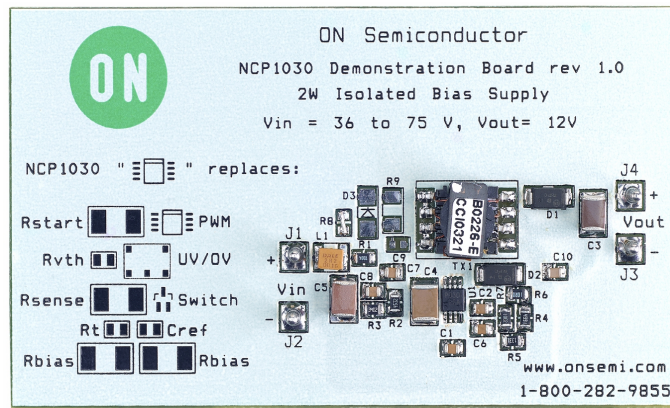
An oscillator frequency of 275 kHz is obtained with a timing capacitor ( $C_T$ ) of 680 pF. The tolerance of  $C_T$  is set at 5%.

## SNUBBER

An RCD snubber as shown in Figure 9 is added to help reduce noise. The snubber is returned to the positive supply rail to reduce the voltage stress on  $C_9$  to  $V_{in}$ . If returned to the negative supply rail, the voltage stress is  $2V_{in}$ .



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**Figure 13. Demonstration Board (Actual Size)**

**Table 4. Bill of Materials**

Ref	Value	Vendor	Part Number
C1	680 pF	Vishay	VJ0805A681JXA
C2	0.033 $\mu$ F	Vishay	VJ0805Y333KXXA
C3	22 $\mu$ F	TDK	C4532X5R1E226M
C4	2.2 $\mu$ F	TDK	C4532X7R1H225M
C5	2.2 $\mu$ F	TDK	C4532X7R2A225M
C6	680 pF	Vishay	VJ0805A681JXA
C7, C8	0.01 $\mu$ F	Vishay	VJ0805Y103KXXAT
C9	100 pF	TDK	C1608C0G2E101J
C10	0.022 $\mu$ F	TDK	C2012X7RE223K
D1, D2	-	ON Semiconductor	MBRA160T3
D3	-	ON Semiconductor	MURA110T3
J1-J4	-	Mill-Max	Terminal
L1	2.2 $\mu$ H	Vishay	IMC-1210
R1	1 M $\Omega$	Vishay	CRCW08051004F
R2	45.3 k $\Omega$	Vishay	CRCW08054532F
R3	34 k $\Omega$	Vishay	CRCW08053402F
R4	4.99 k $\Omega$	Vishay	CRCW08054991F
R5	1.30 k $\Omega$	Vishay	CRCW08051301F
R6	10 $\Omega$	Vishay	CRCW080510R0F
R7	10 k $\Omega$	Vishay	CRCW08051002F
R8	0 $\Omega$	Vishay	CRCW0805000ZJ
R9	499 $\Omega$	Vishay	CRCW12104990F
TX1	-	Coilcraft	B0226-E
U1	-	ON Semiconductor	NCP1030DR2

## DESIGN VERIFICATION

The final step in our design includes validation and test of the bias supply. Before powering the supply, it should be inspected for potential problems. A few suggestions include:

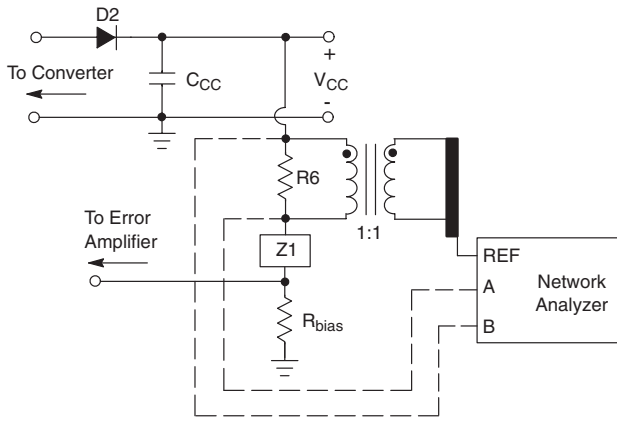
1. Verify all connections. Check for shorts and opens, especially on the input and output terminals.
2. Verify component values.
3. Slowly increase the input voltage while monitoring the input current. If the input current exceeds 10 mA, repeat steps 1 to 3.
4. Once the input voltage reaches 25 V, measure the voltage on critical nodes. The NCP1030 start-up regulator should be ON. If the voltages are not correct, remove power and repeat steps 1 to 3.
5. Increase the input voltage to 36 V. Measure the output voltage. If it is not approximately 12 V, repeat steps 1 to 3.
6. Increase the input voltage above 80 V. The output should turn OFF.

Please be careful when probing and testing the converter. High voltage may be present. Exercise CAUTION!

Once the converter functionality is verified, the board performance is evaluated and compared to our original goals. The evaluation criteria includes:

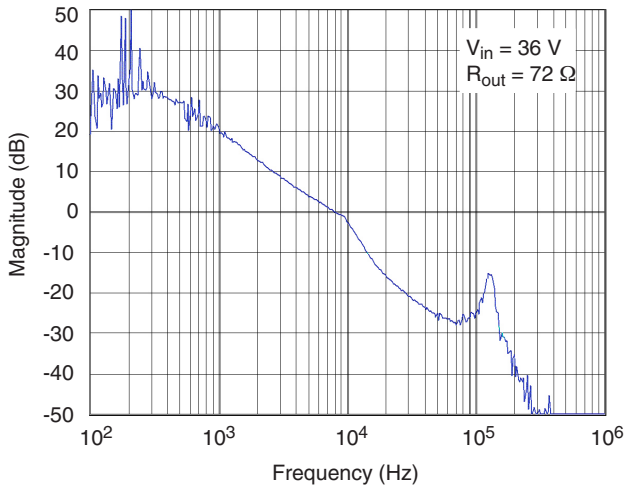
1. Open loop frequency response.
2. Efficiency.
3. Line and load regulation.
4. Step load response.
5. Start-up response.

The open loop response is measured injecting an AC signal across R<sub>6</sub> using a network analyzer as shown in Figure 14.



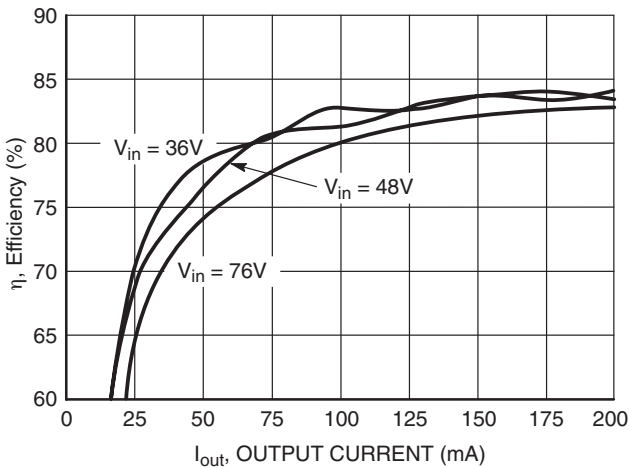
**Figure 14. Open Loop Frequency Response Measurement Set-up**

The measured frequency response is shown in Figure 15. The crossover frequency is measured at 9 kHz.



**Figure 15. Open Loop Frequency Response**

Peak efficiency is measured at 83%. Figure 16 shows the efficiency vs. output current under several input voltage conditions.



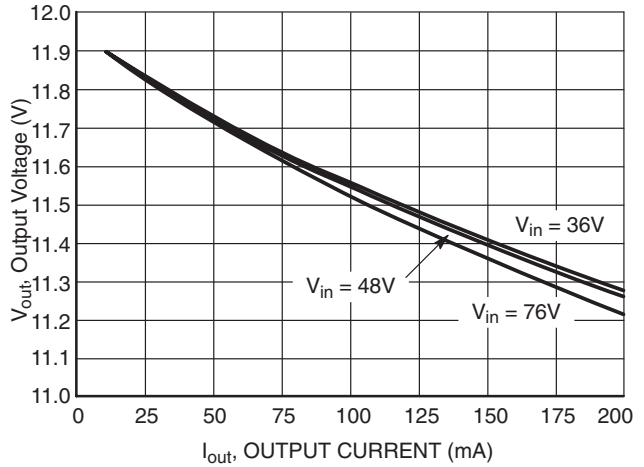
**Figure 16. Efficiency vs Output Current**

Line and load regulation are calculated using Equations 27 and 28, respectively.

$$\text{Reg}_{\text{LINE}} = \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \quad (\text{eq. 27})$$

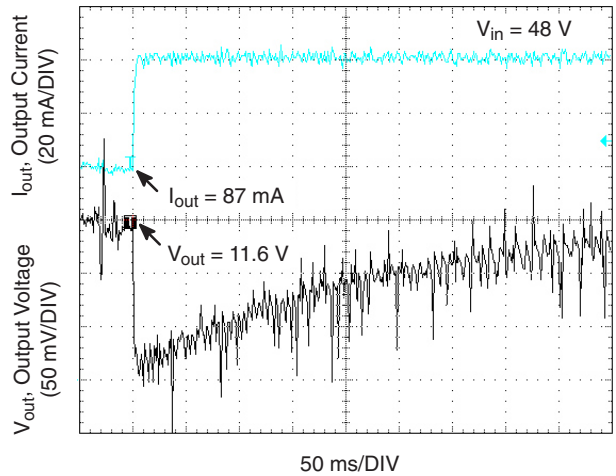
$$\text{Reg}_{\text{LOAD}} = \frac{V_{\text{out}}(\text{No Load}) - V_{\text{out}}(\text{Full Load})}{V_{\text{out}}(\text{No Load})} \quad (\text{eq. 28})$$

Line regulation is measured below 0.5% and load regulation is measured below 8%. Figure 17 shows the output voltage variation to output current under several input voltage conditions.



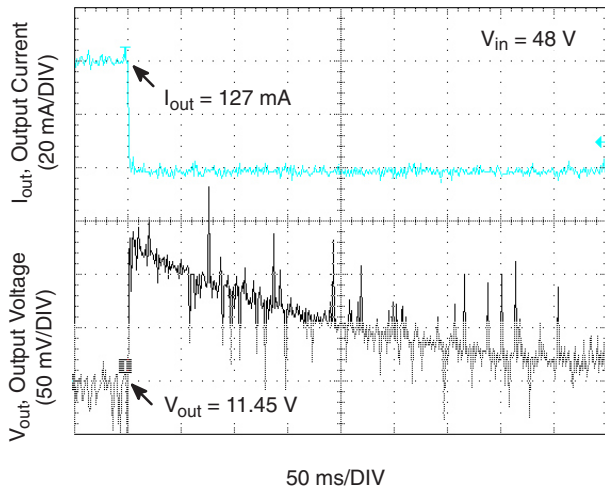
**Figure 17. Output Voltage vs. Output Current**

The dynamic response of the converter is evaluated stepping the load current from 50% to 75% and from 75% to 50% of  $I_{\text{out}}(\text{max})$ . The step load transient responses are shown in Figures 18 and 19.



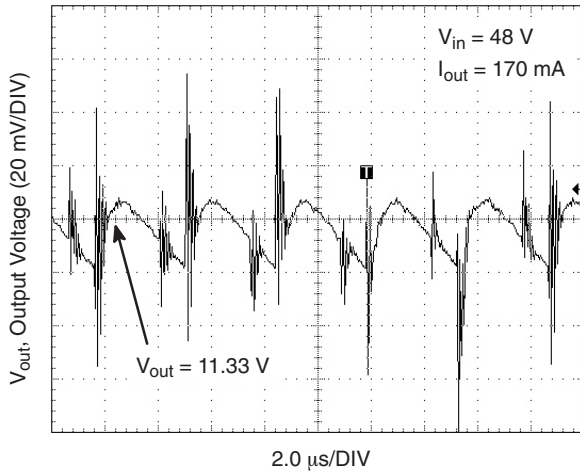
**Figure 18. Output Voltage Response to a Step Load from 87 mA to 127 mA**





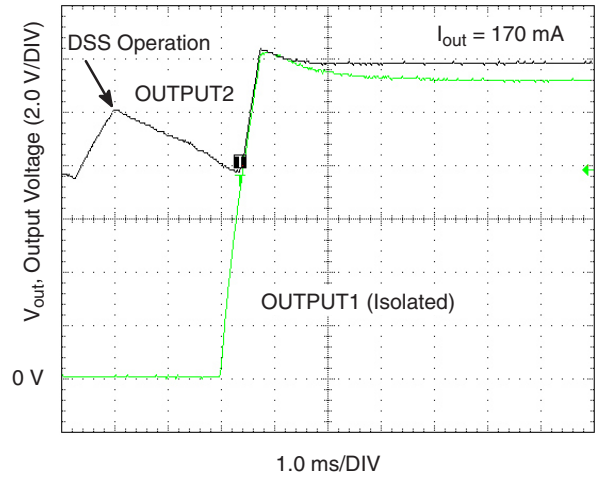
**Figure 19. Output Voltage Response to a Step Load from 127 mA to 87 mA**

Output voltage ripple is measured at 25 mV for an output current of 170 mA. It is significantly below the 50 mV target. The output voltage ripple waveform is shown in Figure 20.



**Figure 20. Output Voltage Ripple**

Finally, the converter turn ON response at full load is evaluated. Figure 21 shows the output turn ON transient response at full load.



**Figure 21. Output Voltage During Turn ON at Full Load**


Output 2 operates in DSS while the converter is disabled. Once the converter is enabled, Output 1 tracks Output 2.

**SUMMARY**

An isolated 12 V bias supply for a 48 V telecom system is implemented using the NCP1030. The converter achieves a peak efficiency of 83% while providing good transient response.

**REFERENCES**

1. Ridley, Ray. "The Evolution of Power Electronics", *Switching Power Magazine*, Fall 2001:16-30.
2. Pressman, Abraham I. *Switching Power Supply Design*. 2nd ed. New York, NY: MacGraw Hill.

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